

# A Fast-Locking All-Digital Phase-Locked Loop with a Novel Counter-Based Mode Switching Controller

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**Abstract**—Settling time is a crucial design issue in Phase-Locked Loop (PLL) used in modern wireless communication systems. A Digitally Controlled Oscillator (DCO)-based multi-operational modes All-Digital PLL (ADPLL), which can achieve an ultra fast settling time of 10  $\mu$ s, has been intensively researched. This paper describes a novel Counter-Based Mode Switching Controller (CB-MSC) for the ADPLL to further reduce its settling time. By monitoring the variation of DCO Tuning Word (OTW), the CB-MSC can control the ADPLL to switch from one operational mode to another quickly, which significantly reduce the mode switching time. An estimated OTW for presetting the DCO is also generated by the CB-MSC to accelerate the frequency acquisition process. The proposed ADPLL was designed in VHDL and simulated in ModelSim environment. Simulation results demonstrate that a minimum settling time of 5.7  $\mu$ s is achieved and the average improvement factor is 37.8%.

**Index Terms**—ADPLL, frequency dithering, fast-locking, mode switching controller, OTW presetting.

## I. INTRODUCTION

Phase-Locked Loop (PLL) is an essential block of modern communication systems, which is used as frequency synthesizer supplying local clock frequency. It is traditionally implemented using a Charge-Pump and a Voltage Controlled Oscillator (VCO), which suffers from high level reference spurs, poor phase noise caused by charge-pump mismatch and large die area due to integrated RC loop filter. Recently, taking the advantage of nanometer-scale CMOS process, several Digitally Controlled Oscillator (DCO)-based All-Digital PLLs (ADPLLs) have been proposed in [1]–[3]. Compared with traditional CPPLL, the ADPLL has many advantages. First, it avoids analog components and can be implemented using automated CAD tools. Second, all the signals in the ADPLL are digital, therefore it is immune to the digital switching noise in SoC system. Third, in the ADPLL, frequency locking is faster than in CPPLLs. As presented in [4]–[6], the settling time is about 20  $\mu$ s to 30  $\mu$ s in CPPLLs, while it achieved 10  $\mu$ s settling time in the ADPLL [7].

Settling time is a key specification of PLL-based frequency synthesizer. For instance, in cellular mobile system, settling time determines how agile a communication channel can be switched from one frequency to another and how fast the system can be turned on or off [8]. For ZigBee application, it is important to minimize energy consumption of the wireless terminal node by minimizing the active duty-cycle, which depends on the settling time of the PLL [9]. A fast settling

process also causes less negative effects on the rest blocks in a System-on-Chip (SoC) environment due to less noise produced by the PLL.

Taking the advantage of nanometer-scale CMOS process, several Digitally Controlled Oscillator (DCO)-based All-Digital PLLs (ADPLLs) have been proposed in [1]–[3], which achieved much faster settling time than classic Charge-Pump PLLs (CPPLLs). A block diagram of the DCO-based ADPLL is shown in Fig. 1. In the ADPLL, to achieve a large output frequency range and a simple control logic, the tunable capacitors in the DCO are split into several banks. Each bank corresponds to an operational mode. The Mode Switching Controller (MSC) is used to control the ADPLL to switch from one mode to another. The total settling time of the multi-operational modes ADPLL consists of the frequency acquisition time in each mode and the mode switching time determined by the MSC. Consequently, fast frequency acquisition and quick mode switching are the approaches to achieve a fast settling time.

Various techniques have been reported to reduce the settling time of ADPLLs. One of the most popular techniques is the dynamic control of system's loop bandwidth. As presented in [10], the loop bandwidth was adjusted during the tracking mode to accelerate the frequency acquisition process. A DCO codeword presetting method using PVT calibration was reported in [11], which enabled one-cycle frequency acquisition. A feed-forward technique which used the input reference signal to compensate the phase error was proposed in [12]. Other techniques such as binary search algorithms and two stages TDC for ADPLL were studied in [13] and [14]. Most techniques focused on the frequency acquisition process but neglected the mode switching process. To the authors' knowledge, there has been no report that focused on the MSC.

This paper presents a fast-locking ADPLL with a novel Counter-Based MSC (CB-MSC), which takes into account both the frequency acquisition process and the mode switching process. By monitoring the variation of DCO Tuning Word (OTW), the CB-MSC can control the ADPLL to switch from one operational mode to another quickly, which significantly reduces the mode switching time. An estimated OTW for presetting the DCO is also generated by the CB-MSC to accelerate the frequency acquisition process. Simulation results demonstrate that the maximum improvement factor is up to

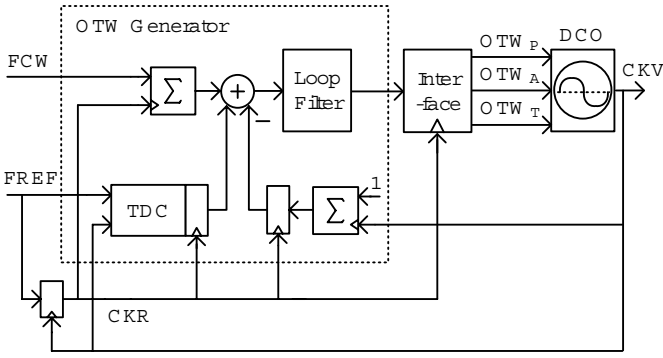


Fig. 1. Block diagram of the ADPLL in [10].

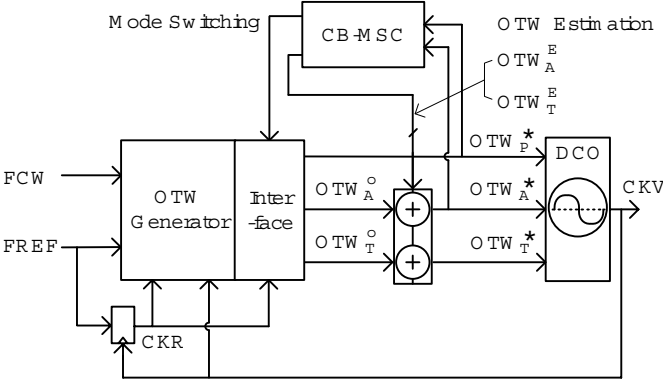


Fig. 2. Block diagram of the proposed fast-locking ADPLL

62.5% compared with [10].

## II. ARCHITECTURE OVERVIEW OF THE PROPOSED FAST-LOCKING ADPLL

The diagram of the proposed fast-locking ADPLL is shown in Fig. 2. The OTW generator is the same as that marked in dotted square in Fig. 1. The tunable capacitors in the DCO are quantized and split into three banks. Each bank corresponds to an operational mode of the ADPLL, namely PVT-calibration ( $P$ ) mode, acquisition ( $A$ ) mode, and tracking ( $T$ ) mode, respectively. The three modes are sequentially activated during the frequency acquisition process of the ADPLL. The DCO output frequency ( $f_{CKV}$ ) is direct set by the  $OTW_X^*$ , where  $X = P, A, \text{ and } T$ .

The proposed CB-MS monitors the variation of  $OTW_X^*$  and generates a mode switching signal and estimated OTWs for the ADPLL. In  $P$  mode,  $OTW_P^*$  is monitored by the CB-MS. When  $P$  mode is completed,  $OTW_P^*$  is fixed, and a mode switching signal is generated to control the ADPLL to switch to  $A$  mode immediately. Also an estimated OTW,  $OTW_A^E$ , is generated and added to the original OTW value ( $OTW_A^o$ ) to preset the DCO, which will greatly accelerate the frequency locking speed in  $A$  mode. The same operation as in  $P$  mode takes place in  $A$  mode.

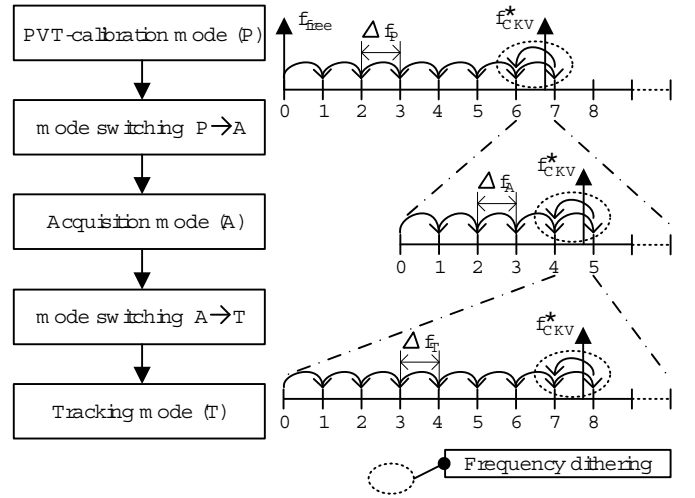


Fig. 3. An example of frequency acquisition process of the ADPLL with frequency dithering.

## III. PRINCIPLE OF THE CB-MS

In the multi-operational modes ADPLL, how to judge that the frequency acquisition process is completed in a certain operational mode is the crucial issue for the MSC. The proposed CB-MS solves this problem basing on the ADPLL's inherent characteristic of frequency dithering, which will be explained in detail in this section.

### A. Frequency Dithering in the DCO-Based ADPLL

Fig. 3 shows an example of frequency acquisition process of the three-operational modes ADPLL. The DCO free running frequency is defined as  $f_{free}$  and the desired output frequency is  $f_{CKV}^*$ , which is determined by the frequency command word (FCW) and frequency reference (FREF) clock. When the frequency acquisition is completed in a certain mode, the DCO output frequency dithers between the upper and lower frequency levels around the frequency desired, which is marked in the dotted circle in Fig. 3. This frequency dithering characteristic of the ADPLL is due to the frequency quantization effect of the DCO. Furthermore, as shown in Fig. 4(a), when the desired output frequency  $f_{CKV}^*$  is close to the upper frequency level  $f_2$ , the time that  $f_{CKV}$  stays at  $f_2$  ( $T_{high}$ ) is longer than the time that at lower frequency  $f_1$  ( $T_{low}$ ). This is because when the DCO output frequency is  $f_2$ , the frequency difference between  $f_2$  and  $f_{CKV}^*$  is very small, therefore, it takes a long time for the ADPLL to accumulate a large enough phase error to change the DCO output from  $f_2$  to  $f_1$ . When the DCO output frequency is  $f_1$ , there is a large frequency difference between  $f_1$  and  $f_{CKV}^*$ , so it takes a short time for the ADPLL to accumulate a phase error that is big enough to change the DCO output back to  $f_2$ . The other two statuses with the similar principles to Fig. 4(a) are shown in Fig. 4(b) and Fig. 4(c).

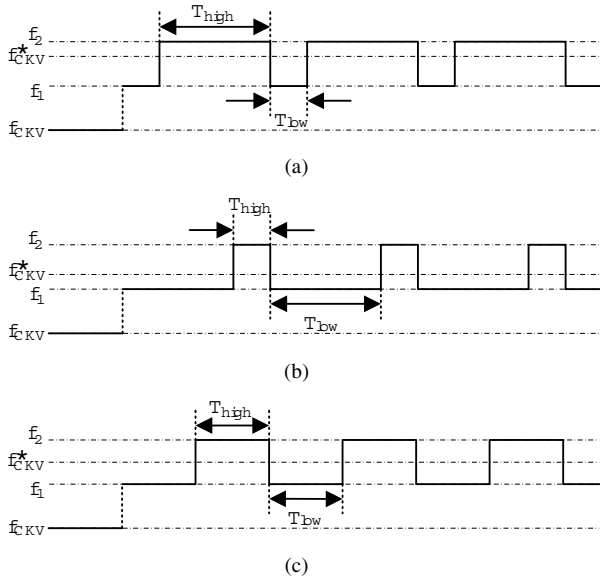


Fig. 4. Three statuses of the desired output frequency between the upper and the lower frequency levels: (a) close to the upper level, (b) close to the lower level, and (c) almost in the middle.

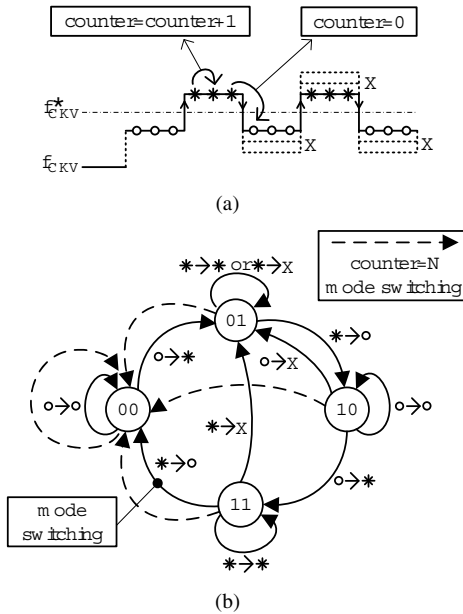


Fig. 5. Principle of the proposed CB-MSC: (a) is a schematic plan of the frequency dithering, (b) is the state switching of the adopted FSM according to (a).

### B. Details of the CB-MSC

The novel CB-MSC is based on the ADPLL's inherent characteristic of frequency dithering. A Finite State Machine (FSM) accompanied by a counter is adopted to realize the proposed CB-MSC. The principle is shown in Fig. 5. The counter is used to record  $T_{high}$  and  $T_{low}$  in  $P$  mode and  $A$  mode. Symbols 'o', '\*', and 'X' represent different frequency levels.

There are two conditions that indicate the frequency acquisition process has been completed in the current operational

TABLE I  
ADPLL SIMULATION PARAMETERS

Reference frequency FREF	13 MHz
DCO free running frequency $f_{free}$	2398 MHz
Frequency command word FCW	23-bit ( $I_{8\text{-bit}} + F_{15\text{-bit}}$ )
Output frequency range	2.4 GHz ~ 2.5 GHz
Loop filter gain	$2^{-6}$
Loop bandwidth	32.328 kHz
TDC resolution	30 ps
$\Delta f_P$	2333 kHz
$\Delta f_A$	397 kHz
$\Delta f_T$	23 kHz
OTW <sub>P</sub>	8 bit
OTW <sub>A</sub>	8 bit
OTW <sub>T</sub>	6 bit

mode and the ADPLL needs to switch to the next operational mode:

- 1) One condition is that the DCO output frequency dithers between two adjacent frequency levels (for example 'o' and '\*') for  $Q$  times. In our design  $Q$  is set to 2. In this condition, the state of the FSM traverses all the available states starting from '00' to '01', '10', '11' sequently and finally back to '00'. Simultaneously, a mode switching signal is generated to instruct the ADPLL to switch to the next operational mode. This condition means that the DCO output frequency stays at neither  $f_1$  nor  $f_2$  for a long time, which corresponds to Fig. 4(c). In this circumstance, the desired frequency  $f_{CKV}^*$  is in the middle of  $f_1$  and  $f_2$ . Consequently, the estimated OTW<sub>A</sub><sup>E</sup> (or OTW<sub>T</sub><sup>E</sup>) is assigned a value in the middle of its available range.
- 2) The other condition is that the counter reaches the upper bound  $N$ , which is 16 in our design. In this condition, the state of the FSM switches to '00' directly and a mode switching signal is generated to instruct the ADPLL to switch to the next operational mode immediately. This condition means the DCO output frequency stays at either  $f_1$  or  $f_2$  for a long time, which corresponds to Fig. 4(a) or Fig. 4(b). In this circumstance, the current DCO output frequency is close to the desired  $f_{CKV}^*$ . Therefore, the estimated OTW<sub>A</sub><sup>E</sup> (or OTW<sub>T</sub><sup>E</sup>) is assigned 0.

It should be noted that the value of  $Q$  should be regarded. In our design,  $Q$  is set to 2. Although a bigger  $Q$  could be used, it would take more time for the ADPLL to switch from one operational mode to another, which increases the settling time and also the circuit complexity. Set  $Q$  to 1 is not recommended. Though it could reduce the mode switching time of the ADPLL, it may cause a wrong judgement of frequency acquisition in some cases.

### IV. IMPLEMENTATION AND SIMULATION RESULTS

The proposed fast-locking ADPLL of Fig. 2 is realized in Very-High-Speed Integrated Circuit Hardware Description Language (VHDL) and simulated in ModelSim environment. The reference frequency clock is 13 MHz and the DCO free running frequency is 2398 MHz with all the OTWs initialized

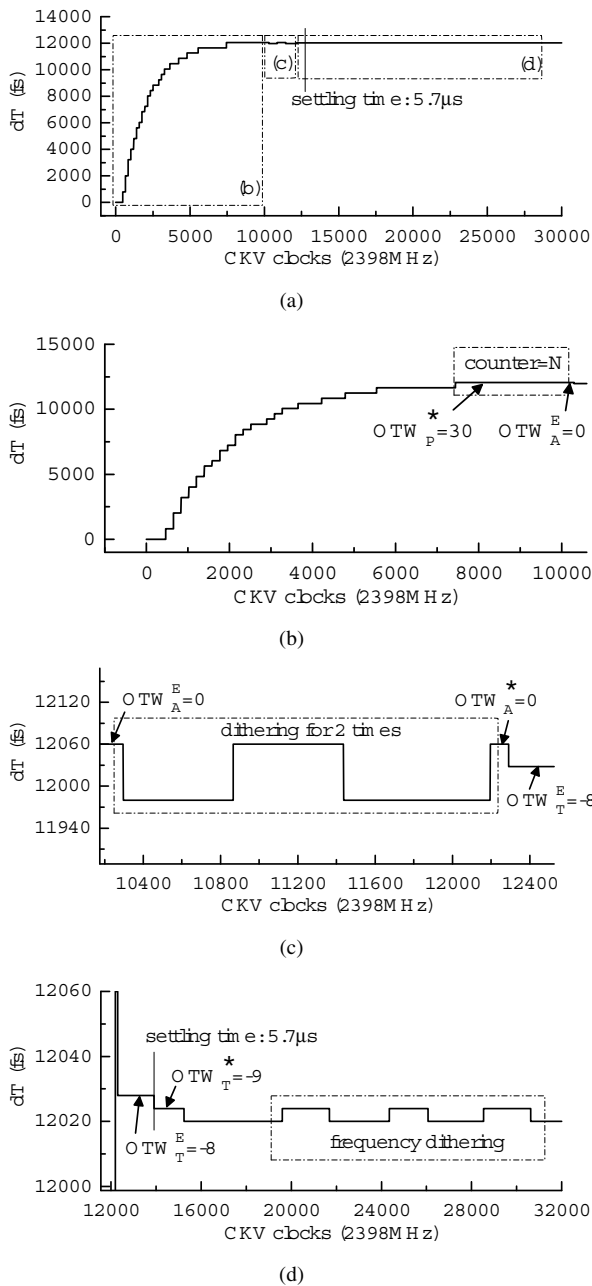


Fig. 6. Transient response of the proposed fast-locking ADPLL with CB-MSC: (a) is the view of whole locking process, (b) is the zoom view of PVT-calibration mode, (c) is the zoom view of acquisition mode, (d) is the zoom view of tracking mode.

to 0. The frequency command word (FCW) is a 23-bit fixed point digital word having 8-bit integer part and 15-bit fractional part. The  $OTW_X$  ( $X = P, A, T$ ) are signed integer with different bits. The detailed parameters of the ADPLL are presented in Table I, which are referenced to those in [10].

#### A. Transient Response of the Proposed ADPLL

An example of frequency acquisition process is given in this part to show the operation details of the proposed CB-MSC.

TABLE II  
SETTLING TIMES OF BOTH ADPLLs AND IMPROVEMENT FACTORS

Frequency (GHz)	Settling Time ( $\mu$ s) T(a) <sup>1</sup>	Settling Time ( $\mu$ s) T(b) <sup>2</sup>	Improvement Factor (%) <sup>3</sup>
2.40	13.7	11.7	14.6
2.41	18.7	8.1	56.7
2.42	14.2	10.2	28.2
2.43	13.6	10.1	25.7
2.44	11.5	8.3	27.8
2.45	12.1	8.3	31.4
2.46	11.6	7.9	31.9
2.47	15.2	5.7	62.5
2.48	12.7	6.3	50.4
2.49	12.9	5.9	54.3
2.50	14.0	9.5	32.1

<sup>1</sup> Settling time of the ADPLL without CB-MSC (Fig. 1).

<sup>2</sup> Settling time of the ADPLL with CB-MSC (Fig. 2).

<sup>3</sup> Obtained by  $(T(a) - T(b))/T(a) \times 100\%$ .

The frequency command word (FCW) is set to 190, therefore, the desired output frequency is 2470 MHz ( $190 \times 13$  MHz). Fig. 6 shows the transient response of the proposed ADPLL. The x-axis is the time evolution in CKV clock units (about 417 ps/cycle). The y-axis is the time deviation expressed in femtoseconds from an initial value of 417 ps, which is the DCO free running cycle. Zoom views of the three operational modes are shown in Fig. 6(b), (c) and (d), respectively.

In PVT-calibration mode, as shown in Fig. 6(b), the DCO output frequency approaches the desired frequency in a step of  $\Delta f_P$  from an initial value of 0. At the end of  $P$  mode, the  $OTW_P$  reaches 30 and remains for a long time. This means that the current DCO output is close to the desired frequency corresponding to Fig. 4(a) or Fig. 4(b). Consequently, the  $OTW_P$  is fixed to 30 and the ADPLL switches to the acquisition mode immediately. According to the principle of the CB-MSC, the estimated  $OTW_A^E$  is assigned 0 for presetting the DCO.

In acquisition mode, the  $OTW_A$  starts from the preset value of  $OTW_A^E$ . In Fig. 6(c), we can see that the frequency dithers between the adjacent frequency levels for 2 times. This means the frequency acquisition process is completed in the current mode according to the principle of the CB-MSC presented in Fig. 5. Therefore, the  $OTW_A$  is fixed to 0 and the estimated  $OTW_T^E$  is assigned -8 based on Fig. 4(c).

In tracking mode, the  $OTW_T$  starts from the preset value of  $OTW_T^E$ , which is very close to the final value  $OTW_T^*$ , as shown in Fig. 6(d). So the frequency acquisition time in this mode is significantly reduced. The total settling time of the ADPLL is 5.7  $\mu$ s. At the end of tracking mode, the frequency is still dithering due to the finite frequency resolution in the DCO. A further finer frequency resolution could be achieved using a  $\Sigma\Delta$  modulator [15].

#### B. Settling Time Improvement

Both the ADPLLs shown in Fig. 1 and Fig. 2 are realized and simulated at different frequency points from 2.4 GHz to 2.5 GHz in a step of 10 MHz. The detailed simulation results are presented in Table II. Settling time comparison and improvement factor are shown in Fig. 7. It can be seen from

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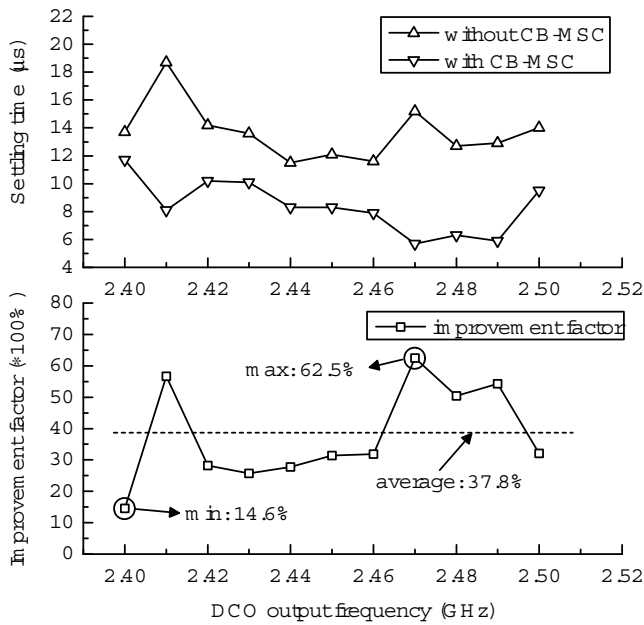


Fig. 7. Settling time comparison of both ADPLLs without and with the proposed CB-MSC.

Fig. 7 that the ADPLL with the proposed CB-MSC achieves a much faster settling time than that without CB-MSC. The average improvement factor is 37.8%. The settling times of the proposed fast-locking ADPLL are less than  $10 \mu\text{s}$  at most frequency points.

There are two reasons for the settling time improvement:

- 1) In our design, both the acquisition mode and tracking mode are considered. While in [10], only the tracking mode is considered. Consequently, a faster acquisition process is achieved in our design.
- 2) A novel CB-MSC is used in our design, which is not contained in [10]. The CB-MSC assists to estimate and preset the OTWs, which greatly reduces the mode switching time and accelerates the locking process in both acquisition mode and tracking mode.

## V. CONCLUSIONS

This paper has presented a novel counter-based mode switching controller for the multi-operational modes DCO-based ADPLL to improve its settling time performance. Since both the frequency acquisition process and the mode switching process are considered, the proposed fast-locking ADPLL achieves a much faster settling time compared with [10]. A minimum settling time of  $5.7 \mu\text{s}$  has been achieved and the average improvement factor is 37.8%. In this work, to achieve a fast frequency acquisition process, estimated OTWs are generated for both the acquisition mode and the tracking mode as shown in Fig. 2. To further reduce the settling time, an estimate  $OTW_P^E$  for presetting the DCO in PVT-calibration mode should be taken into account. How to obtain the  $OTW_P^E$  is a valuable research area and will be our future work.